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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/259,145	02/26/99	PAN	P 3027.1US

EXAMINER	
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ART UNIT	**PAPER NUMBER**
2814	

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JOSEPH A WALKOWSKI
TRASK BRITT & ROSSA
PO BOX 2550
SALT LAKE CITY UT 84110

DATE MAILED: 02/13/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/259,145	PAN ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25,26,31-34,37-40 and 43-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25,26,31-34,37-40 and 43-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☐ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *16* .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed November 28, 2000 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "*free of field oxide structure*".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 25, 26, 31-34, 37-40 and 43-49 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "*free of field oxide structures*" in the application as filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25, 26 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tada (U.S. Patent No. 5,545,577) in view of Koike (5,874,325).

Tada teaches a pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device substantially as claimed including:

a semiconductor substrate (100) free of field oxide structures and having a first surface and a second surface, the first surface opposing the second surface;

at least one p-well (3) and at least one n-well (2) on the substrate first surface;

at least one p-type area (5) within the at least one n-well;

at least one n-type area (6) within the at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer over the substrate first surface. (See Fig. 2c and 3a, col. 6, ll. 3-32).

Thus, Tada is shown to teach all of the features of the claim with the exception of the substantially dopant-free barrier layer is formed extending over the substrate second surface.

However, Koike teaches a substantially dopant-free barrier layer (104) is formed extending over the substrate (101) first and second surface.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the substantially dopant-free barrier layer of Tada extending over the first and second surface as taught by Koike to prevent the second surface from oxidizing.

The pre-anneal intermediate semiconductor substrate of Tada appears to be free of field oxide structures. (See Fig. 2c).

With respect to claim 26, the structure of Tada also includes an oxide layer (4) between the substrate first surface and the substantially dopant-free barrier layer.

With respect to claim 31, the substantially dopant-free barrier layer of Tada is silicon nitride.

4. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tada '577 and Koike '325 as applied to claim 25 above, and further in view of Shim et al. (U.S. Patent No. 5,846,596).

Tada is shown to teach all of the features of the claim with the exception of including silicon oxynitride as the material substantially dopant-free barrier layer.

However, Shim teaches the oxidation resistant layer (130) is formed including silicon oxynitride (130). (See col. 3, ll.18-20).

It would have been obvious to one having ordinary skill in the art at the time of the invention to form the substantially dopant-free, uninterrupted diffusion barrier layer of Tada using silicon oxynitride (130) as taught by Shim because it has an added advantage of oxidation resistance.

5. Claims 33, 34, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tada '577 in view of Koike '325.

Tada teaches a pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device substantially as claimed including:

a semiconductor substrate (100) free of field oxide structures and having a first surface and a second surface, the first surface opposing the second surface;

at least one p-well (3) and at least one n-well (2) on the substrate first surface;

at least one doped area within at least one of the n-well and at least one of the p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer over the substrate first surface. (See Fig. 2c, col. 6, ll. 3-32).

Thus, Tada is shown to teach all of the features of the claim with the exception of the substantially dopant-free barrier layer is formed extending over the substrate second surface.

However, Koike teaches a substantially dopant-free barrier layer (104) is formed extending over the substrate (101) first and second surface.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the substantially dopant-free barrier layer of Tada extending over the first and second surface as taught by Koike to prevent the second surface from oxidizing.

The pre-anneal intermediate semiconductor substrate of Tada appears to be free of field oxide structures. (See Fig. 2c).

With respect to claim 34, the structure of Tada also includes an oxide layer (4) between the substrate first surface and the substantially dopant-free barrier layer.

With respect to claim 37, the substantially dopant-free barrier layer of Tada includes silicon nitride.

With respect to claim 38, the at least one doped area of Tada comprises an impurity selected form the group consisting of a n-type impurity and a p-type impurity.

6. Claims 39, 40 and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tada '577 in view of Koike '325.

Tada teaches a pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device substantially as claimed including:

a semiconductor substrate (100) free of field oxide structures and having a first surface and a second surface, the first surface opposing the second surface;

at least one doped area (2) on the substrate first surface;

at least one second, differently doped area (5) within the at least one first doped area; and

a substantially dopant-free, uninterrupted diffusion barrier layer over the substrate first surface. (See Fig. 2c, col. 6, ll. 3-32).

Thus, Tada is shown to teach all of the features of the claim with the exception of the substantially dopant-free barrier layer is formed extending over the substrate second surface.

However, Koike teaches a substantially dopant-free barrier layer (104) is formed extending over the substrate (101) first and second surface.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the substantially dopant-free barrier layer of Tada extending over the first and second surface as taught by Koike to prevent the second surface from oxidizing.

The pre-anneal intermediate semiconductor substrate of Tada appears to be free of field oxide structures. (See Fig. 2c).

With respect to claim 40, the structure of Tada also includes an oxide layer (4) between the substrate first surface and the substantially dopant-free barrier layer.

With respect to claim 43, the substantially dopant-free barrier layer of Tada comprises silicon nitride.

With respect to claim 44, the at least one first doped area of Tada comprises a p-type impurity (2) and the at least second, differently doped area comprises an n-type impurity.

With respect to claim 45, the at least one first doped area of Tada comprises an n-type impurity (2) and the at least second, differently doped area comprises a p-type impurity.

7. Claims 46-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tada (U.S. Patent No. 5,545,577) in view of Koike (5,874,325).

Tada teaches a pre-anneal intermediate structure in the formation of an isolation structure (9) for a semiconductor device substantially as claimed including:

a semiconductor substrate (100) free of field oxide structures and includes a first surface and a second surface, the first surface opposing the second surface;

at least one p-well (3) and at least one n-well (2) defined on the substrate first surface;

at least one p-type area (5) defined within the at least one n-well;

at least one n-type area (6) defined within the at least one p-well; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over the substrate first surface. (See Fig. 2c, col. 6, ll. 3-32).

Thus, Tada is shown to teach all of the features of the claim with the exception of the substantially dopant-free barrier layer is formed extending over the substrate second surface.

However, Koike teaches a substantially dopant-free, uninterrupted barrier layer (104) is formed extending over the substrate (101) first and second surface. (see Fig. 11).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the substantially dopant-free barrier layer of Tada extending over the first and second surface as taught by Koike to prevent the second surface from oxidizing.

The pre-anneal intermediate semiconductor substrate of Tada appears to be free of field oxide structures. (See Fig. 2c).

Further, it appears that the substantially dopant-free, uninterrupted barrier layer (104) of Koike are formed on both side of the semiconductor substrate (101) thus meet the limitation of "encapsulating".

With respect to claim 47, the pre-anneal intermediate structure of Tada also includes an oxide layer (4) between the substrate first surface and the substantially dopant-free uninterrupted diffusion barrier layer.

With respect to claim 48, the substantially dopant-free uninterrupted diffusion barrier layer of Tada comprises silicon nitride.

8. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tada '577 and Koike '325 as applied to claim 46 above, and further in view of Shim '596.

Tada is shown to teach all of the features of the claim with the exception of including silicon oxynitride as a material for substantially dopant-free barrier layer.

However, Shim teaches the oxidation resistant layer (130) is formed using silicon oxynitride. (See col. 3, ll.18-20).

It would have been obvious to one having ordinary skill in the art at the time of the invention to form the substantially dopant-free, uninterrupted diffusion barrier layer of Tada using silicon oxynitride (130) as taught by Shim because it has an added advantage of oxidation resistance.

Response to Arguments

9. Applicant's arguments filed November 28, 2000 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Regarding the limitation of "free of field oxide structures", the pre-anneal intermediate semiconductor substrate of Tada appears to be *free of field oxide structures*. (See Fig. 2c).

Applicant appears to contend that Tada does not teach a pre-anneal intermediate structure including a substantially dopant-free, uninterrupted diffusion barrier layer. However, it is clear

from Tada that all doping to form wells and doped are already finished prior to forming the barrier layer (nitride). Thus, the nitride barrier layer of Tada is clearly a "substantially dopant-free, uninterrupted diffusion barrier layer". (See col. 6, ll. 20-31).

In response to applicant's argument that although *Koike teaches the deposition of silicon nitride film on both the first and second surfaces of a semiconductor substrate*, the silicon nitride film formed over the first surface is substantially compromised during the formation of field oxide region, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Finally, Shim is cited to show that silicon oxynitride is well known in the art to be used in place of silicon nitride.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
February 8, 2001

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800